IN THE CLAIMS:

Kindly **cancel** claims 1-150, without prejudice.

Kindly **add** the following claims:

151. A controller device for controlling a synchronous dynamic random access memory device, the controller device comprises:

first output driver circuitry to output block size information to the memory device, wherein the block size information defines an amount of data to be output by the memory device; and

input receiver circuitry to receive the amount of data output by the memory device.

152. The controller device of claim 151 further including second output driver circuitry to output an operation code to the memory device, wherein the operation code specifies a read operation and, in response to the operation code, the memory device outputs the amount of data.

153. The controller device of claim 152 wherein the operation code is included in a packet.

154. The controller device of claim 153 wherein the block size information and the operation code are included in the same packet.

155. The controller device of claim 152 wherein the first output driver circuitry outputs the block size information in response to a first transition of an external clock signal and the second output driver circuitry outputs the operation code in response to a second transition of the external clock signal.

156. The controller device of claim 152 wherein the first output driver circuitry and the second output driver circuitry output address information to the memory device.

157. The controller device of claim 156 wherein the block size information, the address information and the operation code are output to the memory device via an external bus.

158. The controller device of claim 157 wherein the external bus includes a plurality of signal lines to carry, in a multiplexed format, the block size information, the operation code and the address information.

159. The controller device of claim 151 further including delay locked loop circuitry, coupled to the input receiver circuitry, to generate an internal clock signal, wherein the input receiver circuitry samples the amount of data in response to the internal clock signal.

160. The controller device of claim 151 further including delay locked loop circuitry, coupled to the first output driver circuitry, to generate an internal clock signal, wherein the first output driver circuitry outputs the block size information in response to the internal clock signal.

161. The controller device of claim 151 wherein the block size information is a binary code.

162. The controller device of claim 151 wherein the input receiver circuitry samples:

a first portion of the amount of data during a first half of a clock cycle of the external clock signal; and

a second portion of the amount of data during a second half of the clock cycle of the external clock signal.

163. The controller device of claim 151 wherein the input receiver circuitry samples:

a first portion of the amount of data in response to a rising edge of the external clock signal; and

a second portion of the amount of data in response to a falling edge of the external clock signal.

164. An integrated circuit device comprising:

a plurality of output drivers to output block size information to a second integrated circuit device, wherein the block size information represents an amount of data to be output by the second integrated circuit device;

a delay locked loop to generate an internal clock signal; and

a plurality of input receivers, coupled to the delay locked loop, to sample the amount of data output by the second integrated circuit device, wherein the amount of data is sampled synchronously with respect to the internal clock signal.

165. The integrated circuit device of claim 164 further including a clock receiver to receive an external clock signal wherein the delay locked loop generates the internal clock signal using the external clock signal.

166. The integrated circuit device of claim 164 wherein the output drivers output the block size information to the second integrated circuit device via a bus, wherein the bus includes a plurality of signal lines.

167. The integrated circuit device of claim 166 wherein the plurality of signal lines carry, in a multiplexed format, an operation code, address information and the block size information.

168. The integrated circuit device of claim 164 wherein the block size information is a binary code.

169. The integrated circuit device of claim 164 wherein the block size information is included in a request packet.

170. The integrated circuit device of claim 169 wherein the amount of data output by the second integrated circuit device is included in a data packet.

171. The integrated circuit device of claim 170 wherein the data packet is output by the second integrated circuit device onto a set of signal lines, and the request packet is output to the second integrated circuit device via the same set of signal lines.

172. The integrated circuit device of claim 164 wherein:

during a first half of a clock cycle of the external clock signal, the plurality of input receivers sample a first portion of the amount of data output by the second integrated circuit device; and

during a second half of the clock cycle of the external clock signal, the plurality of input receivers sample a second portion of the amount of data output by the second integrated circuit device.

173. The integrated circuit device of claim 164 wherein:

the plurality of input receivers sample a first portion of the amount of data output by the second integrated circuit device in response to a rising edge of the external clock signal; and

the plurality of input receivers sample a second portion of the amount of data output by the second integrated circuit device in response to a falling edge of the external clock signal.

174. An integrated circuit device for controlling a synchronous memory device, the controller integrated circuit comprises:

clock receiver circuitry to receive an external clock signal;

delay locked loop circuitry, coupled to the clock receiver circuitry, to generate an internal clock signal; and

a first plurality of output drivers, coupled to the delay locked loop circuitry, to output an amount of data in response to the internal clock signal.

175. The integrated circuit device of claim 174 further including input receivers to sample data that is output by the memory device.

176. The integrated circuit device of claim 175 wherein the input receivers are coupled to the delay locked loop circuitry to sample the data in response to the internal clock signal.

177. The integrated circuit device of claim 174 wherein:

on a rising edge transition of the external clock signal, the input receivers sample a first portion of the data that is output by the memory device; and

on a falling edge transition of the external clock signal, the input receivers sample a second portion of the data that is output by the memory device.

178. The integrated circuit device of claim 174 further including a second plurality of output drivers to output a first operation code to the memory device, wherein the first operation code specifies a read operation, and wherein the memory device, in response to the first operation code, outputs data.

179. The integrated circuit device of claim 174 wherein:

the first plurality of output drivers output a first portion of the amount of data in response to a rising edge transition of the external clock signal; and

the first plurality of output drivers output a second portion of the amount of data in response to a falling edge transition of the external clock signal.

180. The integrated circuit device of claim 174 further including a second plurality of output drivers to output a second operation code to the synchronous memory device, wherein the second operation code specifies a write operation, and wherein the memory device, in response to the second operation code, samples the amount of data.

181. The integrated circuit device of claim 174 wherein the first plurality of output drivers are coupled to the memory device via an external bus that includes a plurality of signal lines.

182. The integrated circuit device of claim 181 wherein the first plurality of output drivers output an operation code and address information to the memory device, in a multiplexed format, via the plurality of signal lines.

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183. The integrated circuit device of claim 174 wherein the first plurality of output drivers include a plurality of output drivers to output an operation code to the memory device, wherein the operation code specifies a read operation, and wherein the memory device outputs data in response to the operation code specifying the read operation.

184. An integrated circuit controller device for controlling a synchronous dynamic random access memory device, the controller device comprises:

a first plurality of output drivers to output block size information to the memory device, wherein the block size information represents an amount of data to be output by the memory device;

a second plurality of output drivers to output an operation code to the memory device, wherein the operation code specifies a read operation, and wherein the memory device outputs the amount of data to the controller device in response to the operation code; and

a plurality of input receivers to receive the amount of data output by the memory device.

185. The controller device of claim 184 wherein the operation code is included in a packet.

186. The controller device of claim 185 wherein the block size information and the operation code are included in the same packet.

187. The controller device of claim 184 wherein the block size information is output in response to a first transition of an external clock signal and the operation code is output in response to a second transition of the external clock signal.

188. The controller device of claim 184 wherein both the first plurality of output drivers and the second plurality of output drivers output address information to the memory device.

189. The controller device of claim 188 wherein the block size information, the operation code, and the address information are output, in a multiplexed format, to the memory device via an external bus.

190. The controller device of claim 184 further including a clock receiver to receive an external clock signal, wherein the first plurality of output drivers outputs the block size information synchronously with respect to the external clock signal.

191. The controller device of claim 190 further including a delay locked loop coupled to the clock receiver and the plurality of input receivers, wherein the delay locked loop generates an internal clock signal, and wherein the plurality of input receivers sample the amount of data in response to the internal clock signal.

192. The controller device of claim 190 further including a delay locked loop coupled to the first plurality of output drivers and the clock receiver, wherein the delay locked loop generates an internal clock signal, and wherein the first plurality of output drivers circuitry outputs the block size information in response to the internal clock signal.

193. The controller device of claim 184 wherein the block size information is a binary code.

194. The controller device of claim 184 wherein:

the plurality of input receivers samples a first portion of the amount of data during a first half of a clock cycle of the external clock signal; and

the plurality of input receivers samples a second portion of the amount of data during a second half of the clock cycle of the external clock signal.